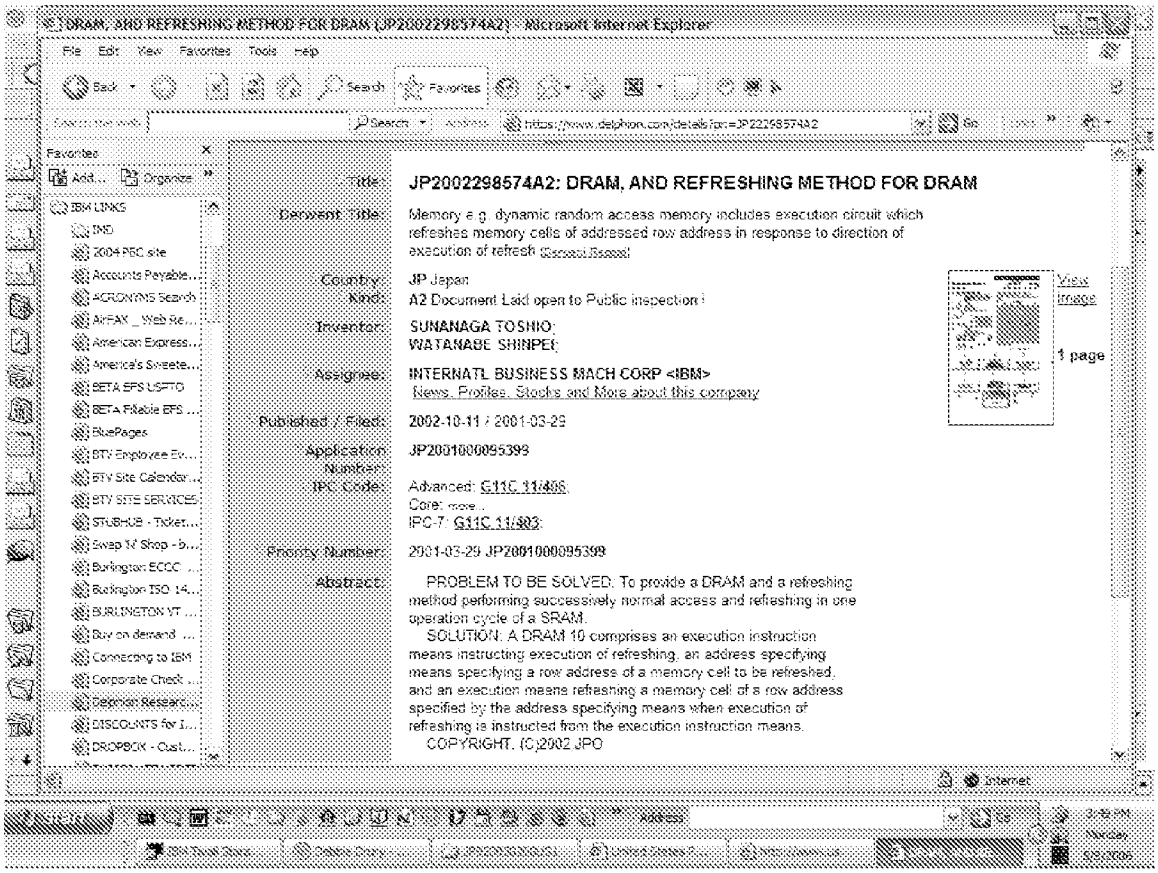

Title: JP2002298574A2: DRAM, AND REFRESHING METHOD FOR DRAM

Derwent Title: Memory e.g. dynamic random access memory includes execution circuit which refreshes memory cells of addressed row address in response to direction of execution of refresh [Derwent Record]

Country: JP Japan
Kind: A2 Document Laid open to Public inspection

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Application Number: JP2001000095399

IPC Code: Advanced: G11C 11/406;
Core: more...
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Priority Number: 2001-03-29 JP2001000095399

Abstract: PROBLEM TO BE SOLVED: To provide a DRAM and a refreshing method performing successively normal access and refreshing in one operation cycle of a SRAM.
SOLUTION: A DRAM 10 comprises an execution instruction means instructing execution of refreshing, an address specifying means specifying a row address of a memory cell to be refreshed, and an execution means refreshing a memory cell of a row address specified by the address specifying means when execution of refreshing is instructed from the execution instruction means.

View image

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